

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

IN THE CLAIMS

The status of the claims is as follows. For the claims that have not been amended in this response, any differences in the claims below and the current state of the claims is unintentional and in the nature of a typographical error.

1. (Previously Presented) A semiconductor apparatus comprising at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor, wherein a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants.

2. (Previously Presented) The semiconductor apparatus as set forth in Claim 1 wherein said at least one double poly bipolar transistor and said at least one double poly metal oxide semiconductor (MOS) transistor comprise a substrate and a first layer of polysilicon (Poly1) material wherein:

said first layer of polysilicon (Poly1) material in said at least one double poly bipolar transistor is doped with impurity ions to form an extrinsic base; and

said first layer of polysilicon (Poly1) material in said at least one double poly MOS transistor is doped with impurity ions to form an MOS transistor gate.

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

3. (Original) The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

4. (Original) The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

5-6. (Cancelled)

7. (Original) The semiconductor apparatus as set forth in Claim 2 wherein:

said substrate is implanted with impurity ions to form an intrinsic base in said at least one double poly bipolar transistor; and

said substrate is simultaneously implanted with impurity ions to form a lightly doped drain in said at least one double poly MOS transistor.

8. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said lightly doped drain in said at least one double poly MOS transistor is self aligned.

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

9. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

10. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

11.-12 (Cancelled)

13. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor and said at least one double poly metal oxide semiconductor (MOS) transistor further comprise a second layer of polysilicon (Poly2) material wherein:

said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor is doped with impurity ions to form an emitter; and

said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor is simultaneously doped with impurity ions to form an MOS source/drain.

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

14. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said emitter in said at least one double poly bipolar transistor is self aligned to an extrinsic base of said at least one double poly bipolar transistor.

15. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said MOS source/drain in said at least one double poly MOS transistor is self aligned to a gate of said at least one double poly MOS transistor.

16. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor is simultaneously doped with impurity ions to form a deep collector.

17. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said MOS source/drain in said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor is etched to separate said MOS source/drain into a source and a drain.

18.-19 (Cancelled)

20. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

21. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

22. (Withdrawn) A method for manufacturing a semiconductor apparatus comprising at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor, said method comprising the steps of:

manufacturing said at least one double poly bipolar transistor in said semiconductor apparatus; and

simultaneously manufacturing said at least one double poly metal oxide semiconductor (MOS) transistor in said semiconductor apparatus.

23. (Withdrawn) The method as set forth in Claim 22 further comprising the steps of:

applying a first layer of polysilicon (Poly1) material to a substrate of said semiconductor apparatus;

doping said first layer of polysilicon (Poly1) material in said at least one double poly bipolar transistor with impurity ions to form an extrinsic base; and

simultaneously doping said first layer of polysilicon (Poly1) material in said at least one double poly MOS transistor with impurity ions to form an MOS transistor gate.

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

24. (Withdrawn) The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

25. (Withdrawn) The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

26. (Withdrawn) The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

27. (Withdrawn) The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

28. (Withdrawn) The method as set forth in Claim 23 further comprising the steps of:

implanting said substrate with impurity ions to form an intrinsic base in said at least one double poly bipolar transistor; and

simultaneously implanting said substrate with impurity ions to form a lightly doped drain in said at least one double poly MOS transistor.

29. (Withdrawn) The method as set forth in Claim 28 wherein said lightly doped drain in said at least one double poly MOS transistor is self aligned.

30. (Withdrawn) The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

31. (Withdrawn) The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

32. (Withdrawn) The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

33. (Withdrawn) The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

34. (Withdrawn) The method as set forth in Claim 28 further comprising the steps of:

applying a second layer of polysilicon (Poly2) material to said at least one double poly bipolar transistor and to said at least one double poly metal oxide semiconductor (MOS) transistor;

doping said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor with impurity ions to form an emitter; and

simultaneously doping said second layer of polysilicon (Poly2) material in said at least one double poly metal oxide semiconductor (MOS) transistor with impurity ions to form an MOS source/drain.

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

35. (Withdrawn) The method as set forth in Claim 34 wherein said emitter in said at least one double poly bipolar transistor is self aligned to an extrinsic base of said at least one double poly bipolar transistor.

36. (Withdrawn) The method as set forth in Claim 34 wherein said MOS source/drain in said at least one double poly MOS transistor is self aligned to a gate of said at least one double poly MOS transistor.

37. (Withdrawn) The method as set forth in Claim 34 further comprising the step of:

simultaneously doping said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor with impurity ions to form a deep collector.

38. (Withdrawn) The method as set forth in Claim 34 further comprising the step of:

etching said MOS source/drain in said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor to separate said MOS source/drain into a source and a drain.

DOCKET NO. P05792
SERIAL NO. 10/777,012
PATENT

39. (Withdrawn) The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

40. (Withdrawn) The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

41. (Withdrawn) The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

42. (Withdrawn) The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.